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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,491	09/23/2003	Robert Sheffield	57983.000131	1242

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EXAMINER	
VAN, LUAN V	

ART UNIT	PAPER NUMBER
1724	

MAIL DATE	DELIVERY MODE
07/13/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/667,491	SHEFFIELD ET AL.	
	Examiner	Art Unit	
	LUAN VAN	1724	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24* is/are allowed.

6)☒ Claim(s) *1,2,4-6 and 19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 31, 2011 has been entered.

Response to Amendment

Claims 1, 2, 4-6, and 19-24 are pending in the application.

Status of Objections and Rejections

All rejections from the previous office action are withdrawn in view of Applicant's amendment. New grounds of rejection under 35 U.S.C. 103(a) are necessitated by the amendments.

Claim Objections

Claims 23 and 24 are objected to because of the following informalities: claims 23 and 24 are duplicates of claim 2, since claim 2 already recites reducing the surface roughness by one of electroplating or vacuum depositing conductive material. It is suggested that the applicant amend claims 23 and 24 to depend on claim 2. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 2, 4-6, and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US patent 4959507) in view of Nagai et al. (US pub 2002/0155021) and Daigle et al. (US 5046238).

Regarding claims 1 and 21-22, Tanaka et al. teaches a method for forming a bonded ceramic-metal composite substrate, the method comprising the step of: providing a layer of the circuit board 1 having the conductive circuit trace 2 (figure 1) on a surface thereof; and reducing a surface roughness (column 2 lines 23-35) of at least one surface of the conductive circuit trace on the surface of the circuit board layer. The method of Tanaka et al. would improve performance of a signal transmitted via the conductive circuit trace, since the surface roughness of the copper element 2 is reduced. Furthermore, Tanaka et al. teaches that the median surface roughness of the copper circuit sheet be not greater than 1 µm, or equivalent to about 254 microinches, and a maximum surface roughness be not greater than 8 µm, or equivalent to about 387 microinches (column 3 lines 9-12).

Tanaka et al. differs from the instant claim in that the reference does not explicitly teach the smaller roughness of the instant claim, or laminating the circuit board with another circuit board layer.

Nagai et al. teaches that "[l]arge surface roughness of a copper foil results in the skin effect such that the current of electric signal having 1 GHz or more of frequency locally flows only on the surface of a coil. As a result, the impedance increases and the

transmission of high-frequency signals is seriously influenced. Fine surface roughness is, therefore, necessary for conductive material used in a high-frequency circuit. The present inventors examined the relationship between the surface roughness and the high-frequency performance and discovered that 2 micrometer or less of surface roughness [or equivalent to about 80 microinches] in terms of the terms of the ten-point average surface-roughness (Rz) attains the desired high-frequency performance. The fine roughness can be provided by means of producing a wrought copper foil or electro-deposited copper foil under appropriate conditions, or chemically or electrolytically polishing the surface of a copper foil" (paragraph 28).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have reduced the surface roughness in the copper sheet of Tanaka et al., because a smaller surface roughness would improve the high-frequency performance of the device by reducing the impedance, as taught by Nagai et al. (paragraph 28).

Daigle et al. teaches a method of fabricating multilayer circuits by laminating a plurality of circuit layers comprised of a dielectric substrate having a circuit formed thereon (Fig. 1-6).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have further modified the method of number 1 by laminating the ceramic substrate with another circuit layer, as taught by Daigle et al., because it would enable the formation of a multilayer circuit board. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have polished the

circuit pattern before laminating since it would not be possible to polish the circuit pattern in the interior of the multilayer laminate.

Tanaka et al. is also silent to whether the etching treatment or polishing is performed laterally or transversely with respect to the circuit pattern.

However, since polishing laterally or transversely with respect to the circuit pattern are the only two possible directions, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have tried polishing the circuit pattern of Tanaka et al. either laterally or transversely in order to improve the reliability of the circuit board, as suggested by Tanaka et al. (column 1 lines 43-51). Given only two choices, it would have been obvious to one having ordinary skill in the art to polish either laterally or transversely as these represent a finite number of predictable polishing directions.

Regarding claim 2, Tanaka et al. teaches wherein the step of reducing the surface roughness includes mechanical polishing the at least one surface (column 4 lines 59-64).

Regarding claims 4-5, the grounds of rejection of the instant claims parallel that given above in claim 1.

Regarding claim 6, Tanaka et al. teaches wherein the at least one surface of the conductive circuit trace includes one of a group consisting of: a surface parallel and distal to a surface of the circuit board; a surface parallel and proximal to the surface of the circuit board; and a surface perpendicular to the surface of the circuit board (figure 1).

Regarding claim 19, Tanaka et al. teaches wherein the conductive circuit trace is formed on the surface of the circuit board layer 1 (figure 1).

Regarding claim 20, Tanaka et al. teaches wherein the conductive circuit trace 2 is bonded (i.e., affixed, column 3 lines 56-60) to the surface of the circuit board layer 1.

Regarding claim 23, since the copper foil or copper sheet is formed by electroplating having the fine roughness, as taught by Nagai et al. (paragraph 28), the surface roughness is reduced by electroplating.

Allowable Subject Matter

Claim 24 is allowed.

Claim 24 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Tanaka et al. teaches polishing by mechanical polishing and chemical polishing, and Nagai et al. teaches electroplating a copper foil having the fine roughness. However, the prior art does not teach or suggest reducing the surface roughness by vacuum depositing conductive material on the at least one surface of the conductive circuit trace.

Response to Arguments

In the arguments presented on page 9 of the amendment filed on May 31, 2011, the applicant argues that Tanaka and Nagai do not teach the limitation of reducing the

surface roughness of the first circuit board layer prior to lamination to a second circuit board layer. The examiner acknowledges that Tanaka does not teach a multilayer circuit board, therefore Daigle is now relied on to teach a laminating process to form a multilayer circuit board. The combination of Tanaka and Daigle would necessarily require that polishing of the circuit trace is performed prior to laminating since the circuit trace would be inaccessible after lamination.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUAN V. VAN whose telephone number is (571)272-8521. The examiner can normally be reached on M-F 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Luan V Van/
Primary Examiner, Art Unit 1724
July 8, 2011